**SRM UNIVERSITY**

**DATE= 13-01-2021**

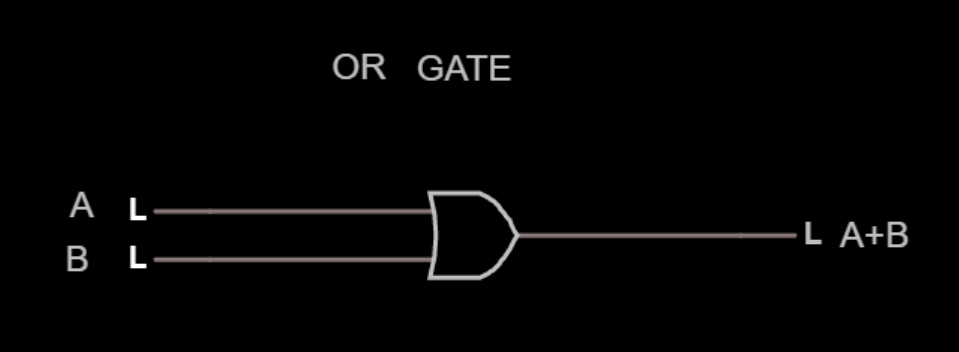
Digital Logic Fundamental

RA2031241010065 (VINEET)

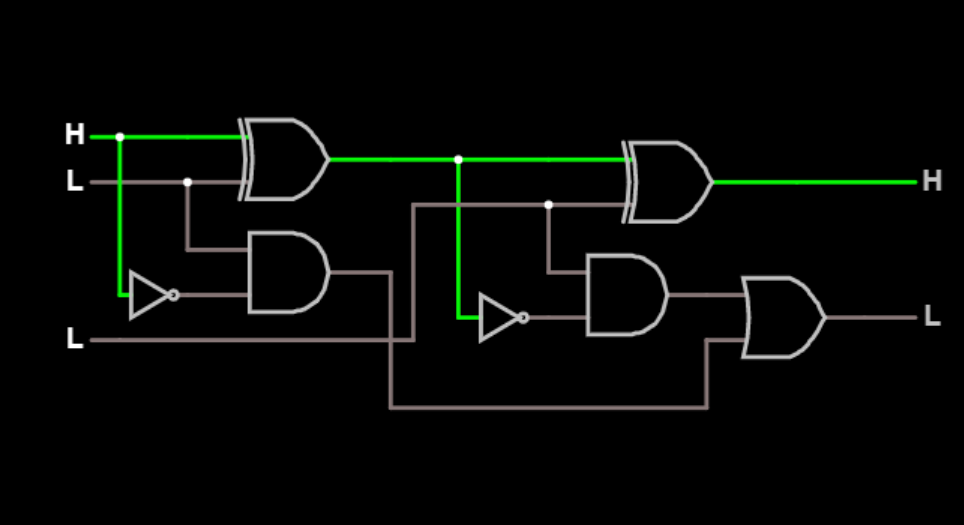
1/13/2021

Session: Logic Gates

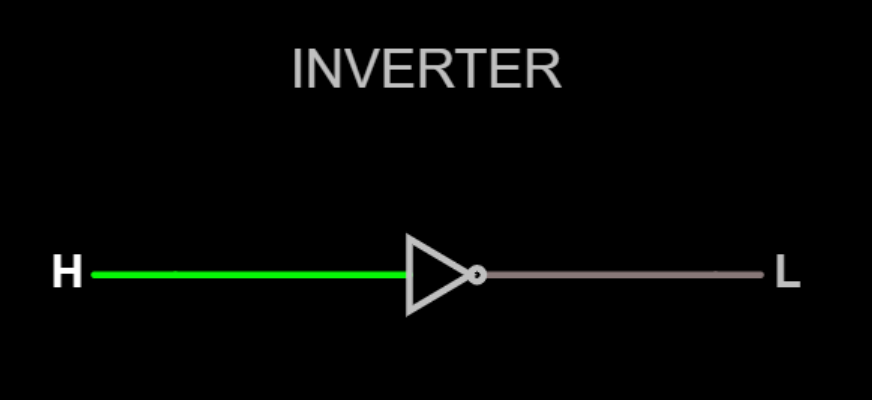
* **Problem Description:** Design a two input OR Gate and verify its functions



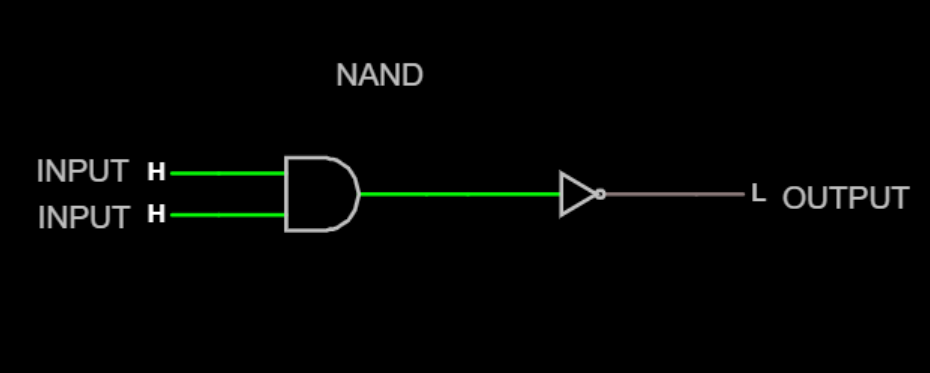
###### Problem Description: Implement a Full Subtractor using two Half Subtractors and an OR gate. Using Logic gates only.



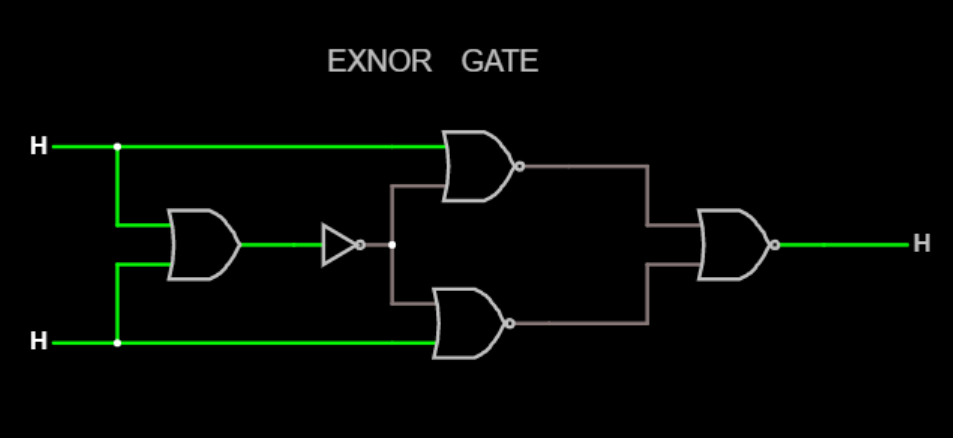
* Problem Description: Design a single input Inverter and verify its results.



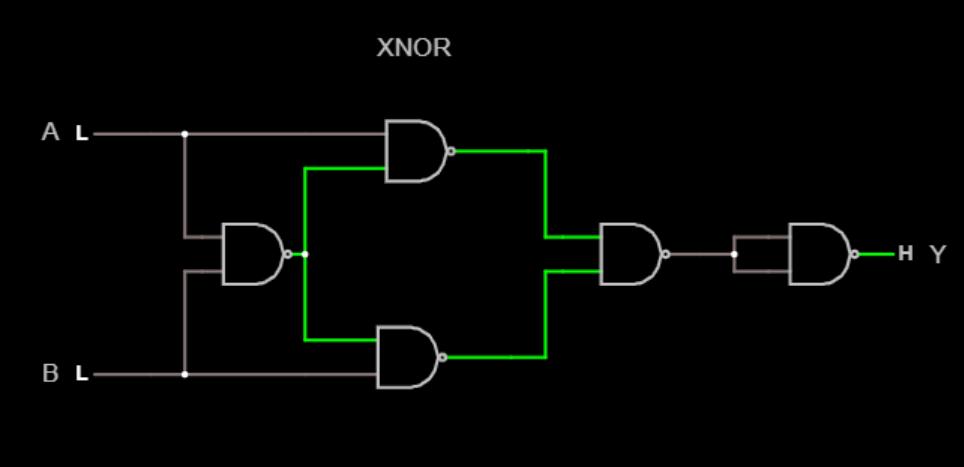
* Problem Description: Design a two input NAND Gate using AND gate chip and verify its functions



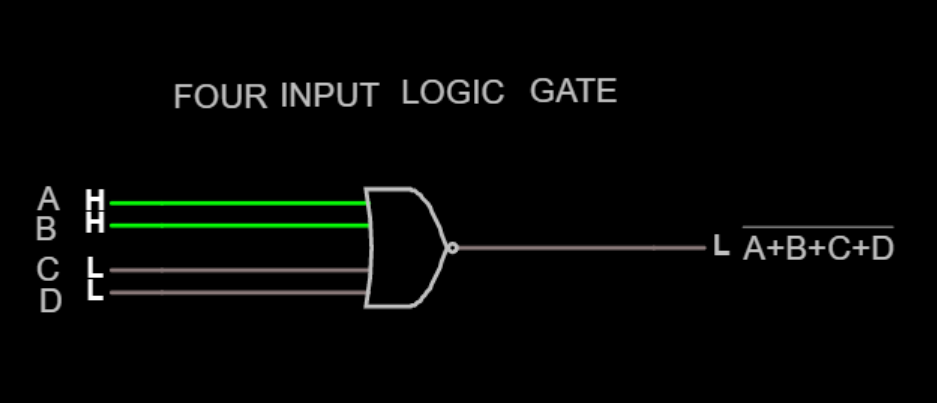
* Problem Description: Design the EXNOR gate using OR and NOR logic



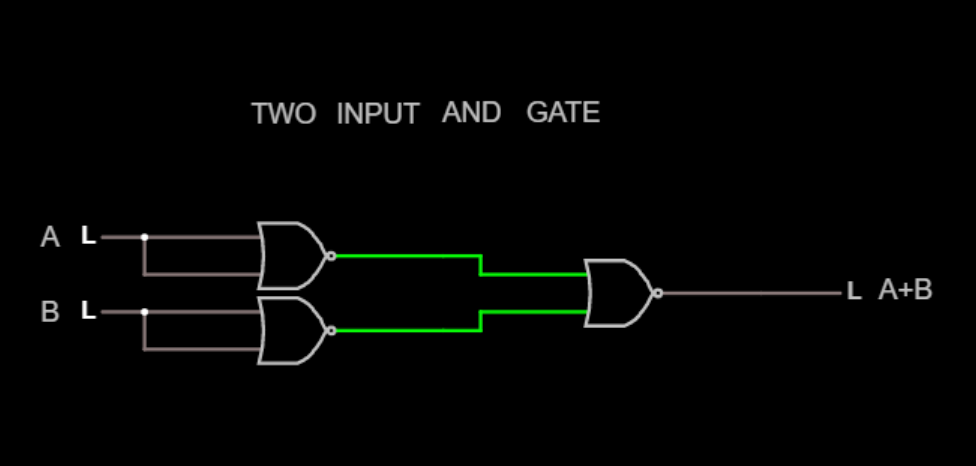
* Problem Description: Design a XNOR gate logic using only NAND gates.
* Note: A, B are inputs and Y will be the output



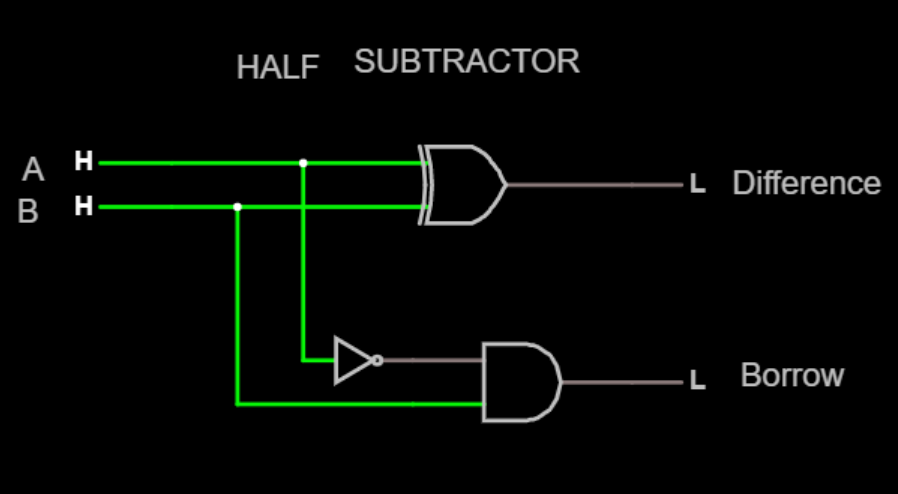
* Problem Description: Design a four Input digital logic gate that returns “High” again when all of its inputs are at a logic level “Low”



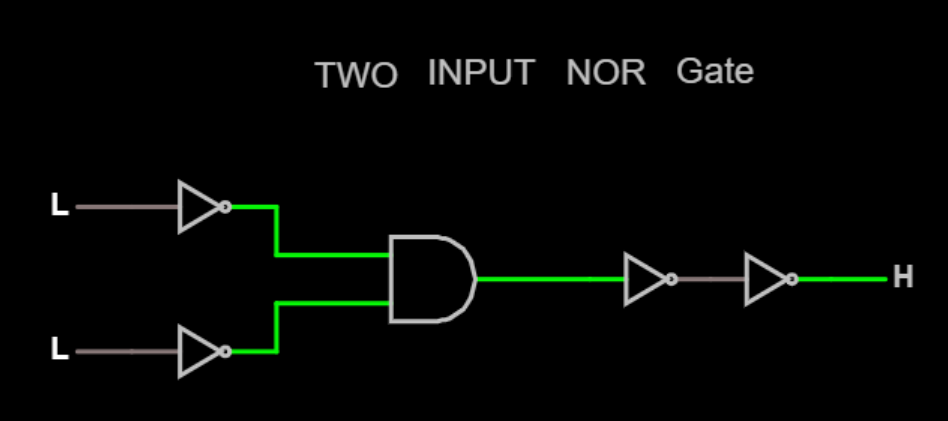
* Problem Description: Design a two input AND gate using NOR logic. Note: A, B are inputs and Y will be the output



* Problem Description: Design half subtractor using basic logic gates

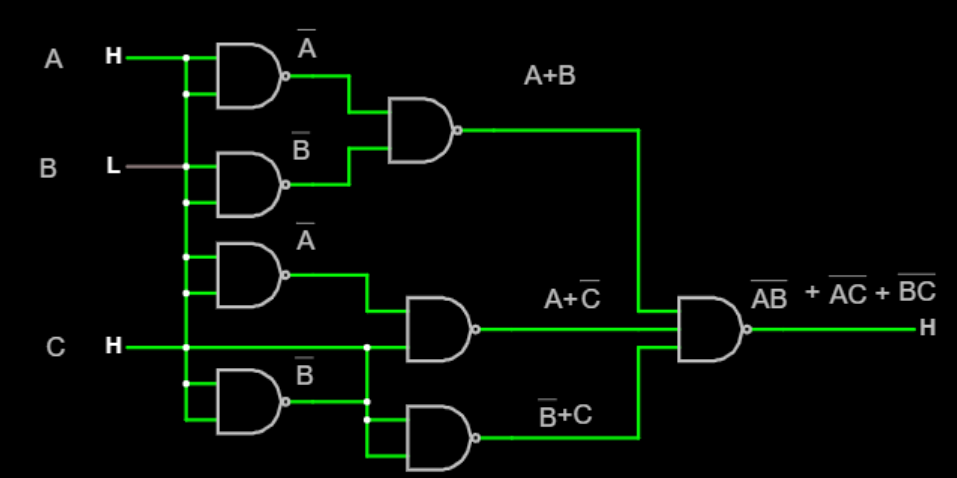


* Problem Description: Design a two input NOR Gate using AND gate chip and verify its functions

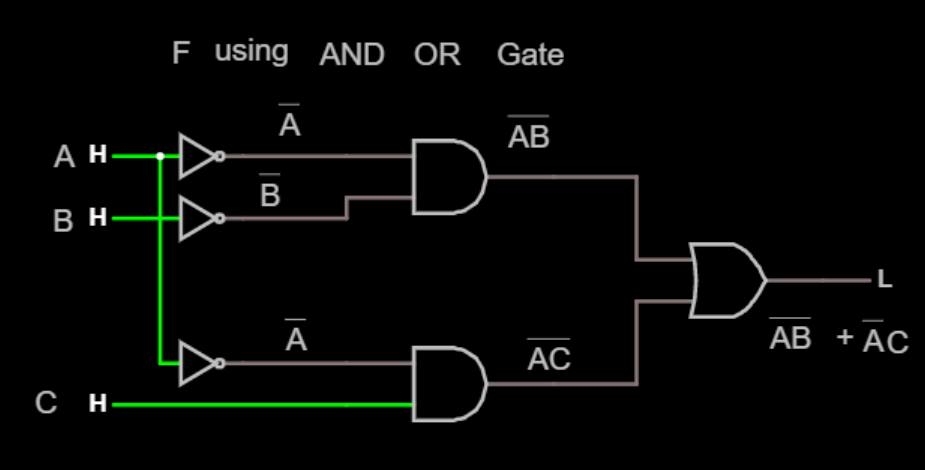


Session: Minimization

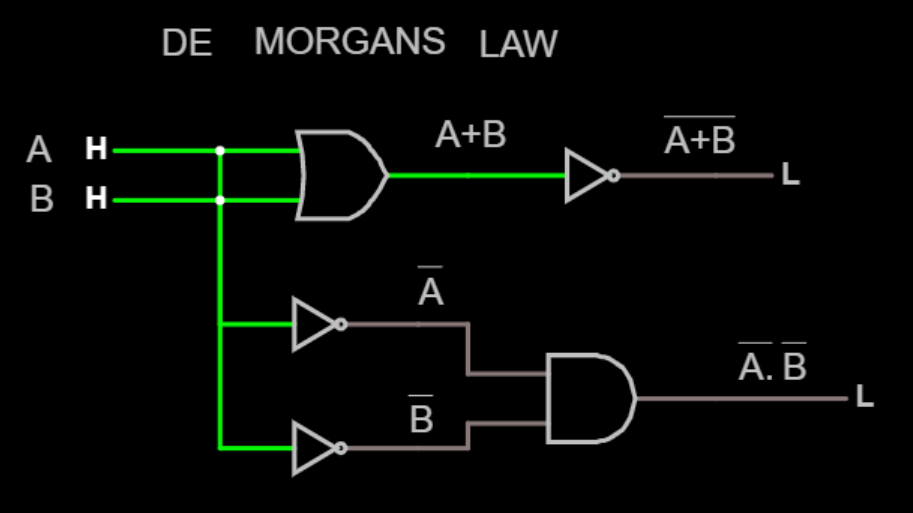
* Problem Description: Draw the Logic diagram for the following for the following expression  F = A′B′ + A′C + B′C​ using NAND and NAND Logic



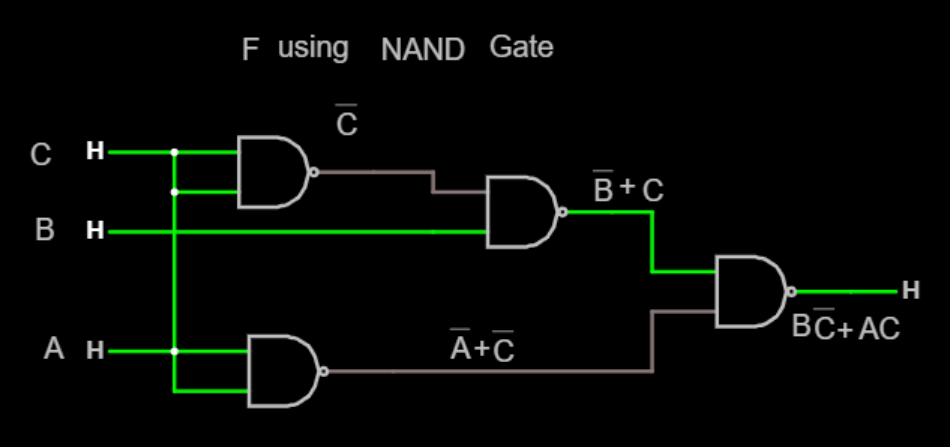
* Problem Description: Draw the Logic diagram for the following for the following expression F=A¯ B¯ + A¯C using AND & OR Logic



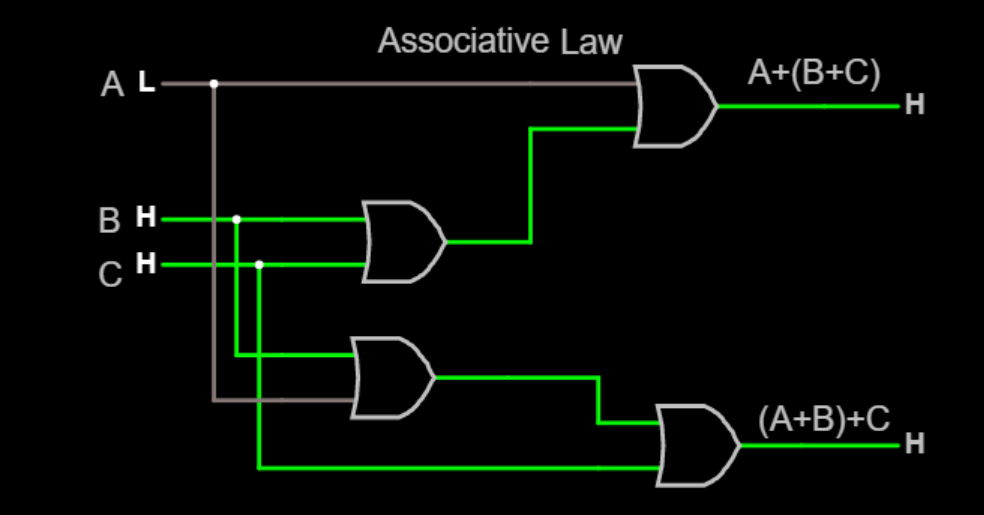
* Problem Description: Implement the De Morgans Law of Boolean Algebra.  
  Note: you must draw Left hand side and Right hand side of the equation A+B¯¯¯=A¯.B¯



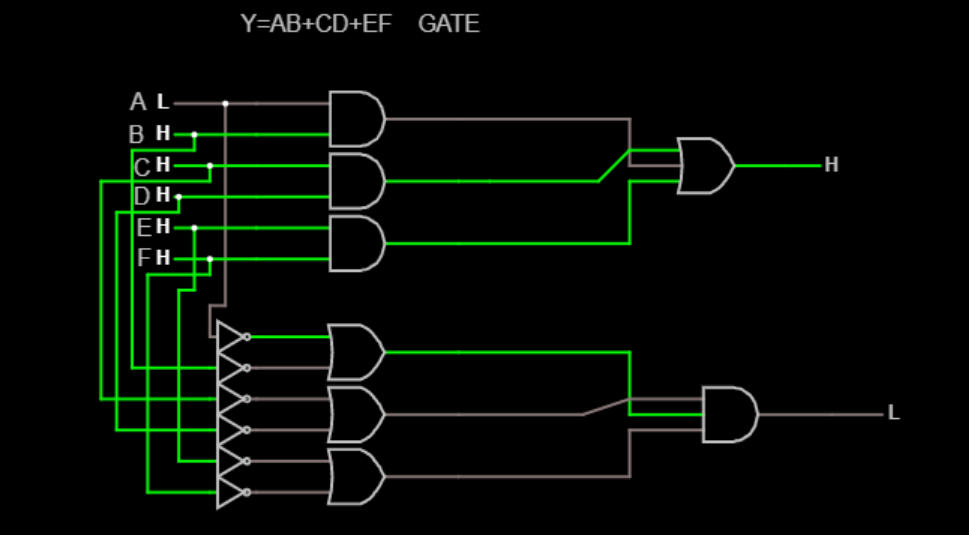
* Problem Description: Draw the Logic diagram for the following for the following expression F=BC¯ + AC​ using NAND and NAND Logic



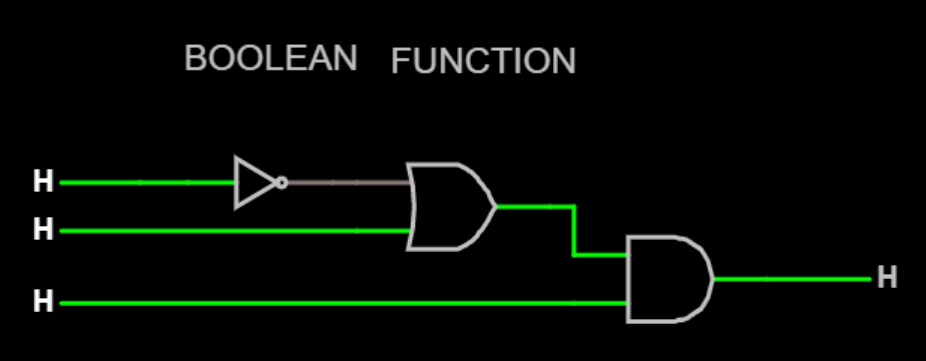
* Problem Description: Implement the Associative law of addition of Boolean Algebra.  
  Note: you must draw Left hand side and Right Hand side of the equation



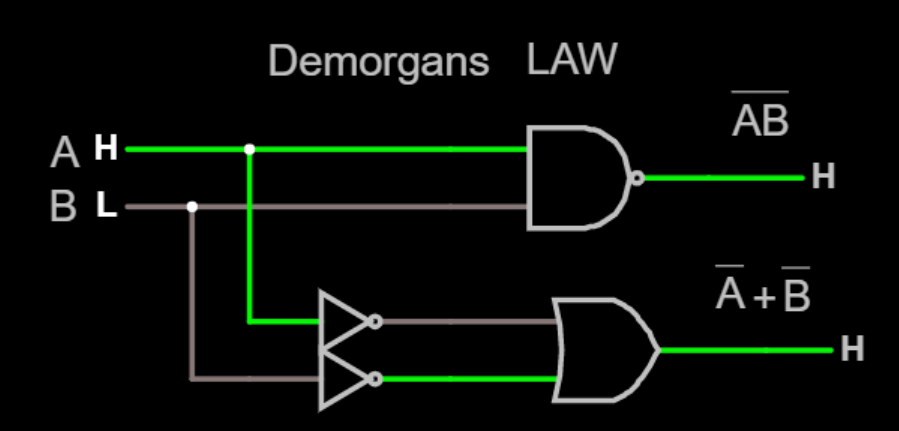
* Problem Description: Draw the Logic diagram for the Complement of Boolean function of Y=AB+CD+EF​.  
  Note: The logic diagram must have two logic diagrams that will take same input source. First diagram should be for the function Y=AB+CD+EF​ and the second diagram would be the inverse function of F. Refer Figure.



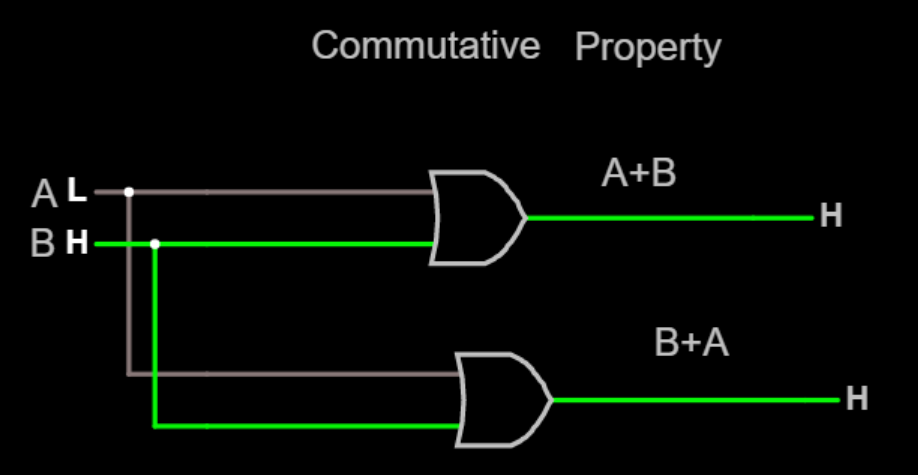
* Problem Description: Implement the Boolean Function with AND - OR logic for the function F = (A¯+B)C​



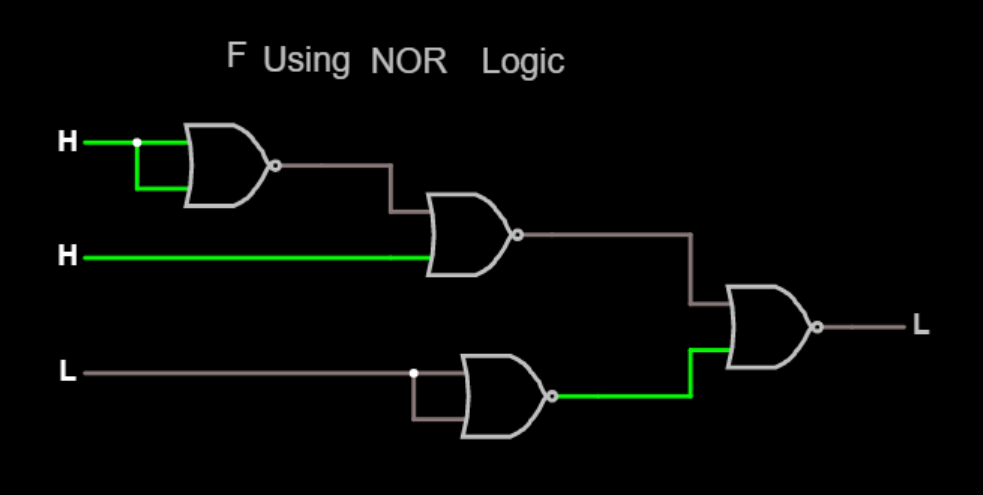
* Problem Description: Implement the De- Morgans Law of Boolean Algebra.  
  Note: you must draw Left hand side and Right hand side of the equation

(AB) ¯= A¯+B¯

* Problem Description: Implement the Commutative property of Boolean Algebra.  
  Note: you must draw Left hand side and Right Hand side of the equation

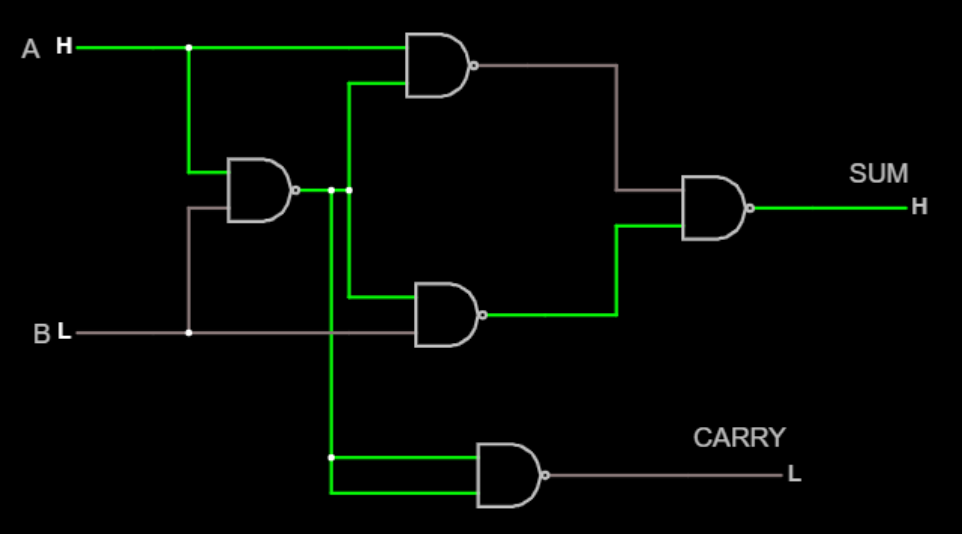


* Problem Description: Implement the Boolean Function with logic NOR-NOR for the function F=(A¯+B)C

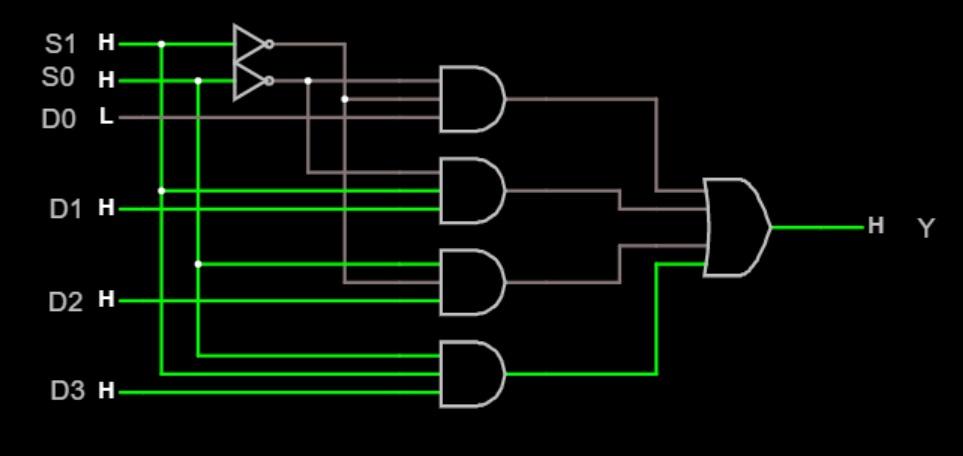


Session: Combinational Circuits

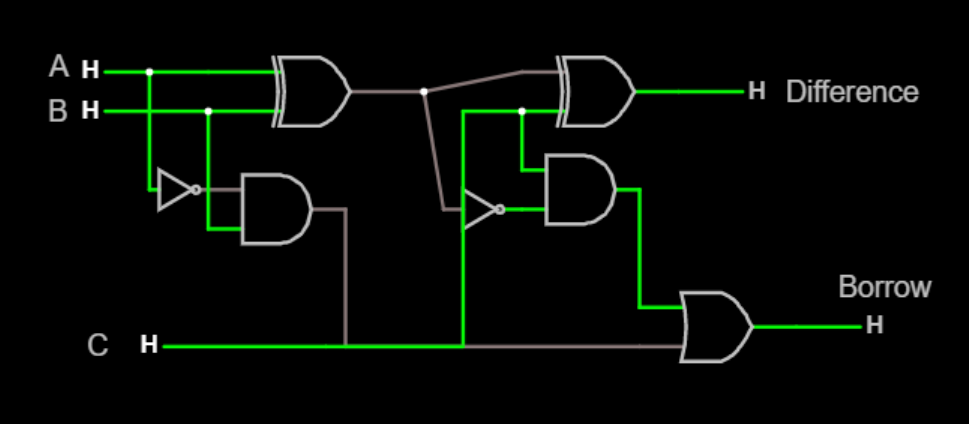
* Problem Description: Design the Half Adder using NAND gates



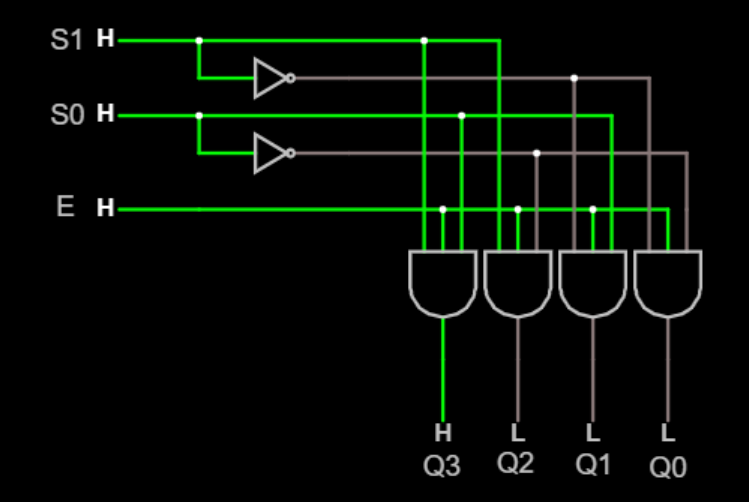
* Problem Description: Design a 4 to 1 Line Multiplexer circuit using Logic gates  
  Hint: The inputs would be of E (Enable), S1 and S0.  
  Output would be Y.  
  The value of Y would be D0 = 00, D1 =01, D2 =10, D3=11



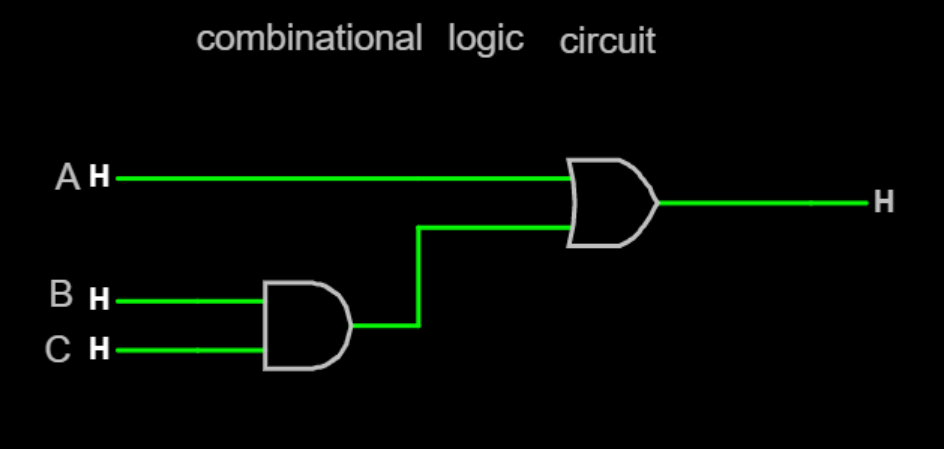
* Problem Description: Design the subtractor circuit that has 2 half adder circuits



* Problem Description: Implement the 1:4 De multiplixer Use Input as E(Enable), Q, so, s1 and Outputs are Q0, Q1, Q2, Q3

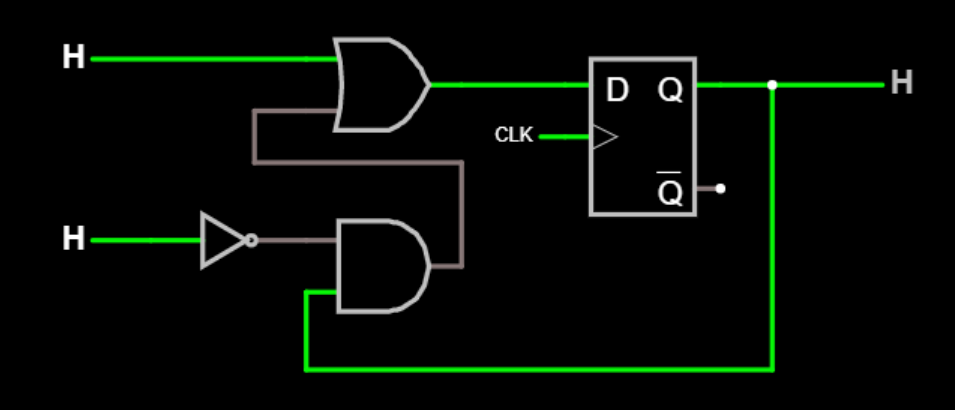


* Problem Description: Design a combination logic circuit with three input variables that will produce a logic 1 output when more than one input variables are logic 1

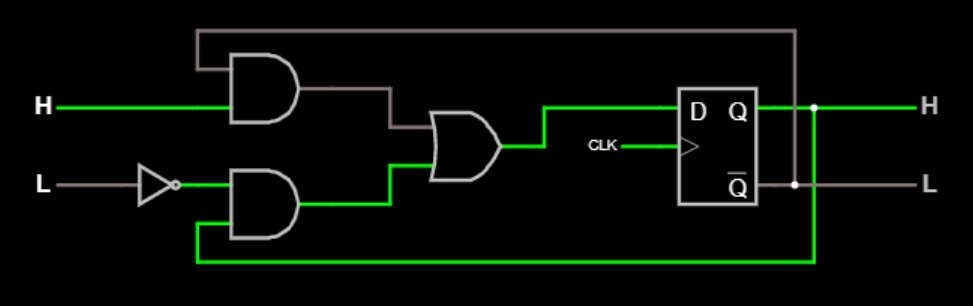


Session: FLIP FLOPS

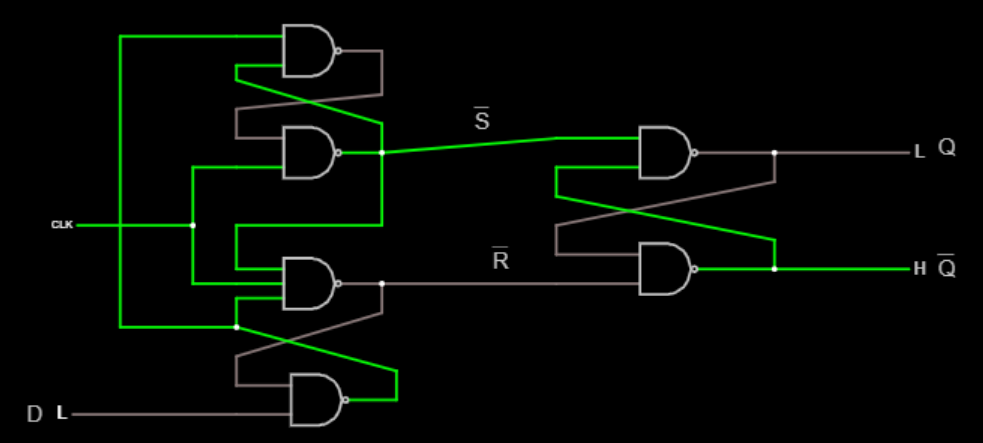
* Problem Description: Raju has DFF, he wants to construct SET-RESET Flipflop help him to construct.



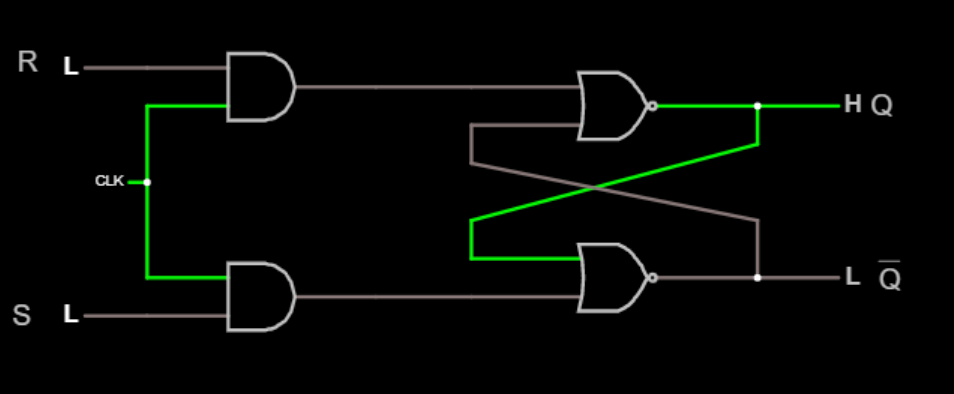
* Problem Description: Construct a JK flipflop using D flipflop



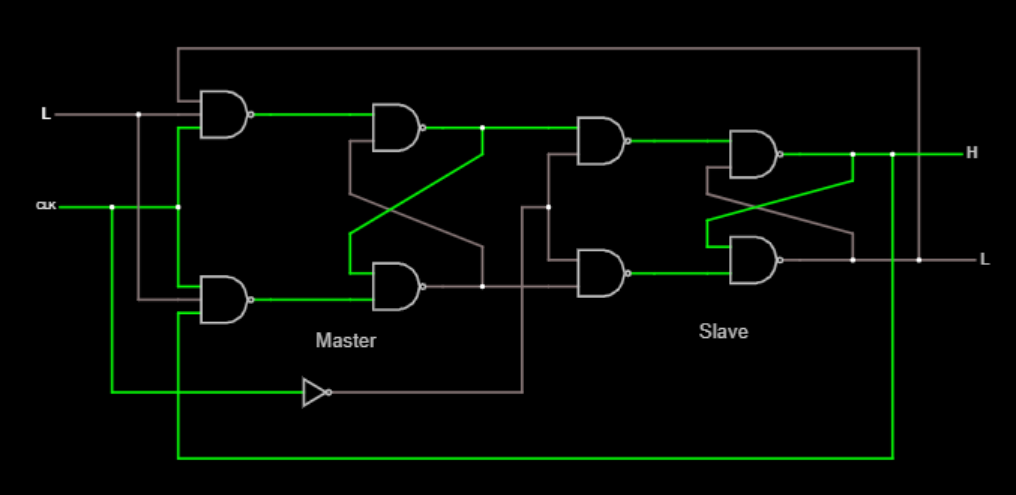
* Problem Description: Construct an Edge triggered delay flipflop



* Problem Description: Design a SR flipflop only using nor and and gate.

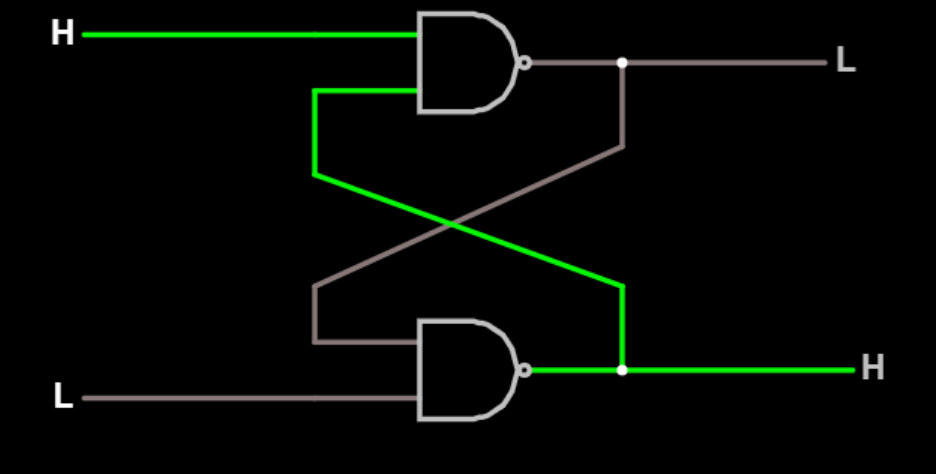


* Problem Description: Build a master slave flipflop using NAND gates.

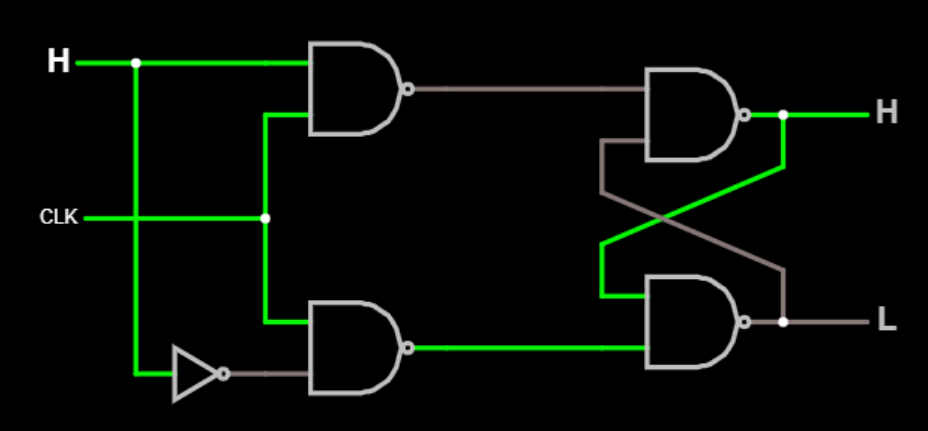


* Problem Description: Construct Set-Reset flipflop without using clock.  
  HINT: Input-S,R

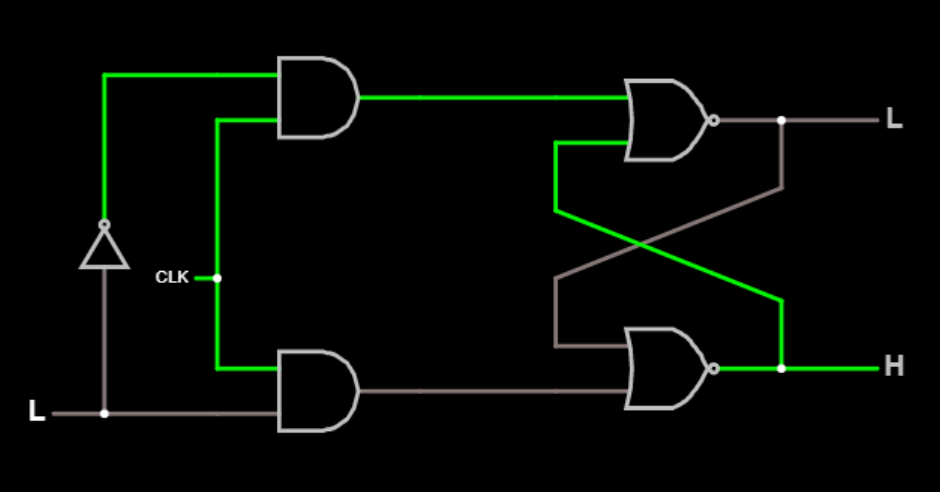
Output-Q, Q'



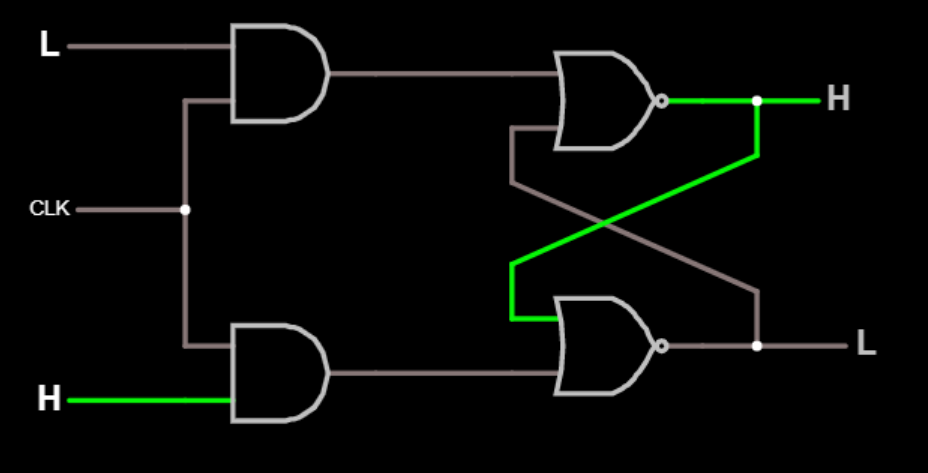
* Problem Description: Srini requires a Delay in his Flipflop help him to build that module using logic gates only.



* Problem Description: Build a D flipflop.



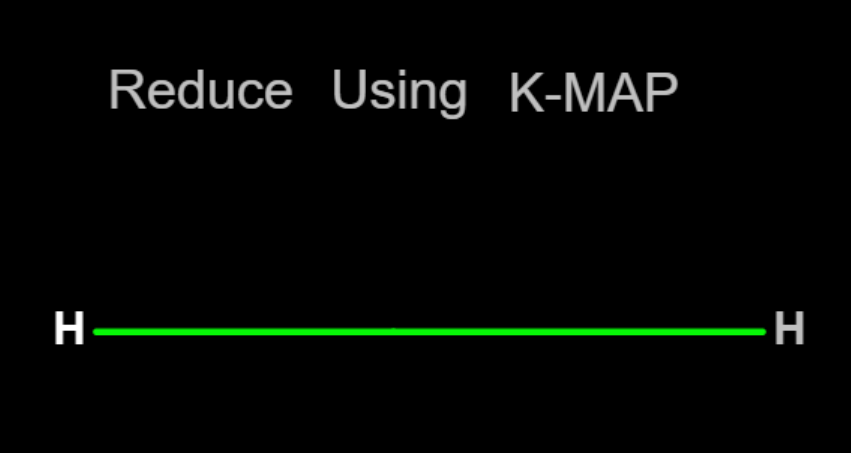
* Problem Description: Construct a Clocked SET-RESET Flipflop.



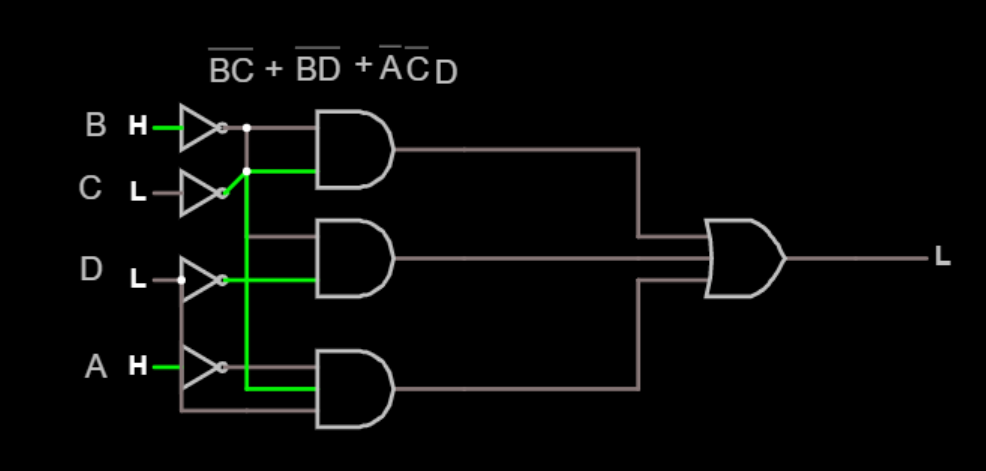
Session: K-MAP

* Problem Description: Draw the reduced logic diagram for

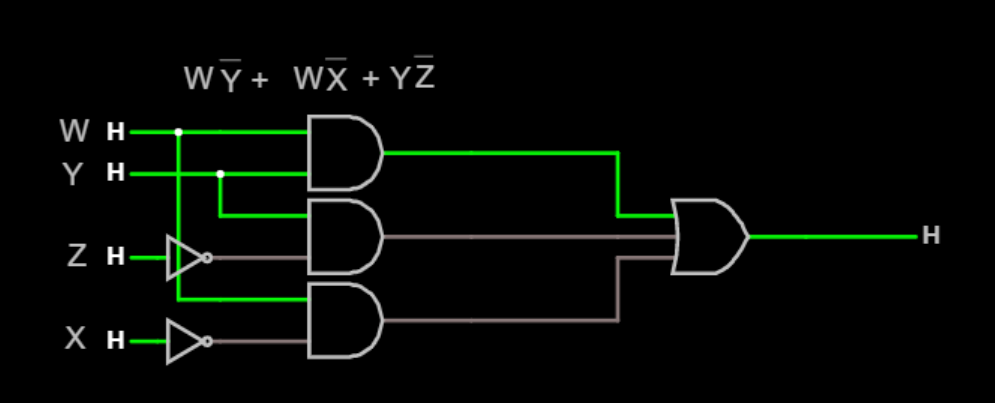
f(A,B,C,D)=∑m(5,6,7,12,13)​+d(4,9,14,15)



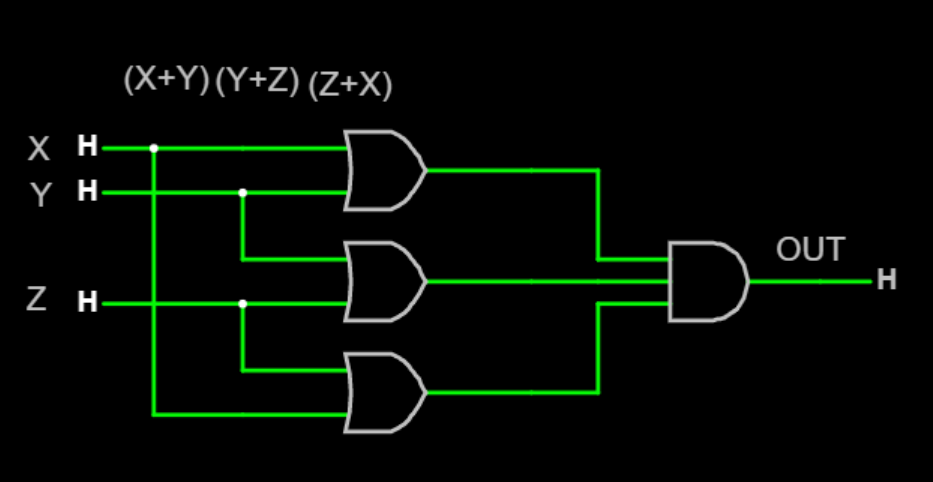
* Problem Description: Find the reduced sum of products using K-MAP F(A,B,C,D)=∑(0,1,2,5,8,9,10)​



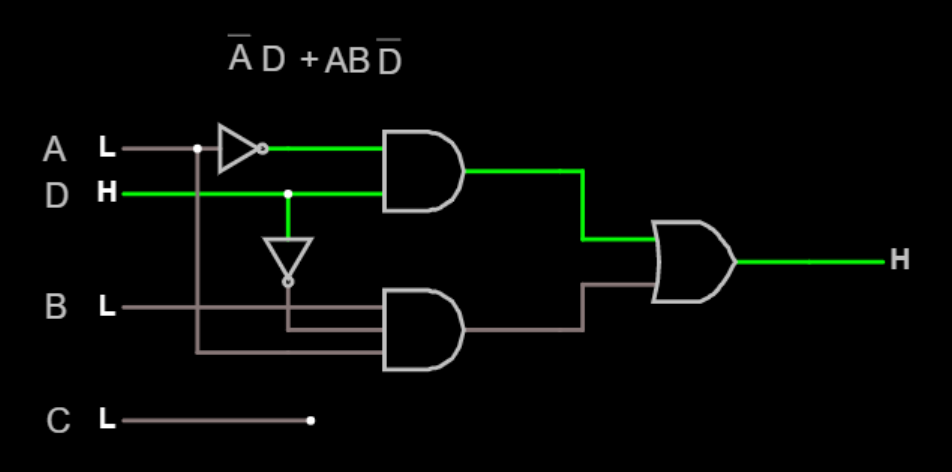
* Problem Description: simplify the following Boolean function, f(W,X,Y,Z) =W X¯Y¯+ WY + W¯YZ¯¯ using K-map.



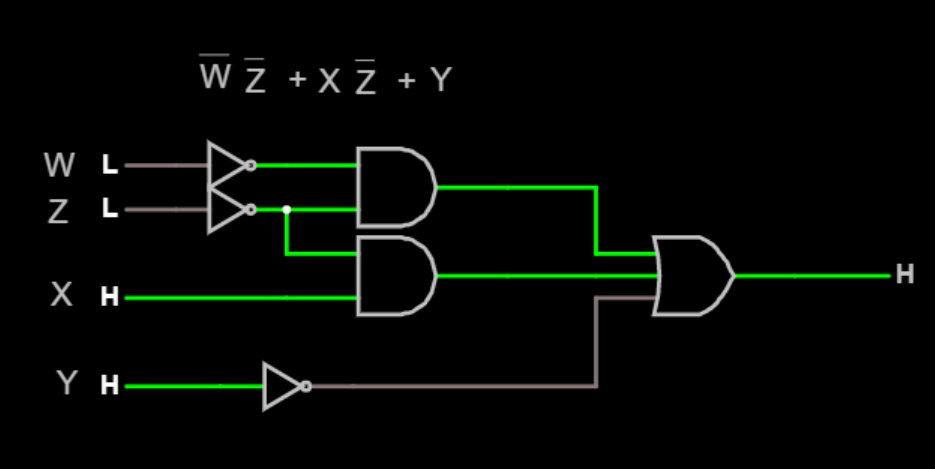
* Problem Description: simplify the following Boolean function, f(X,Y,Z) =πm(0,1,2,4) using K-map.



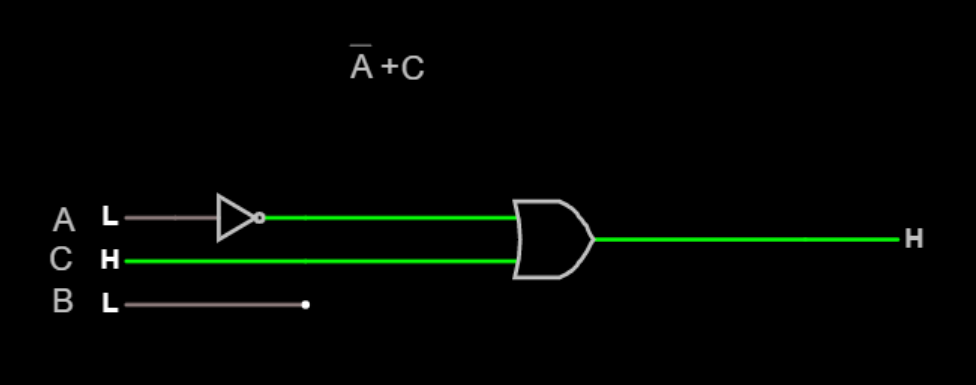
* Problem Description*: Reduction in K-MAP* f*(*A*,*B*,*C*,*D*)=*AB¯¯D*+*ABCD¯¯*​+*A¯BD*+*ABCD¯¯

**

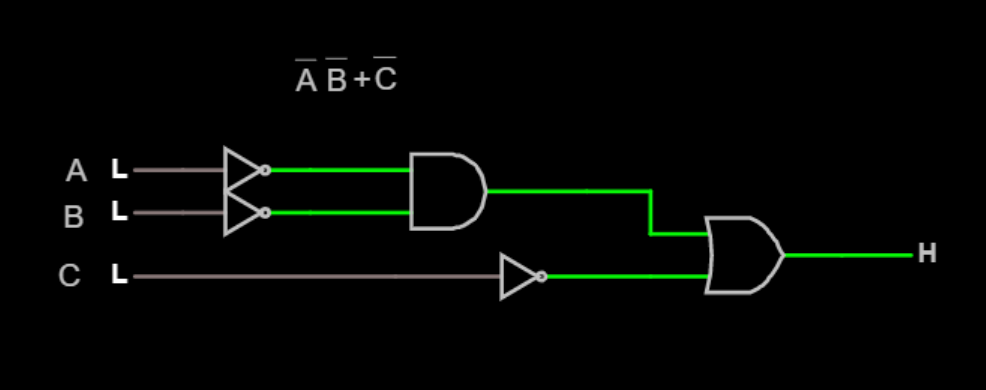
* Problem Description*:* Simplify the following function *F*(*w*,*x*,*y*,*z*)= ∑(​0,1,2,4,5,6,8,9,12,13,14)



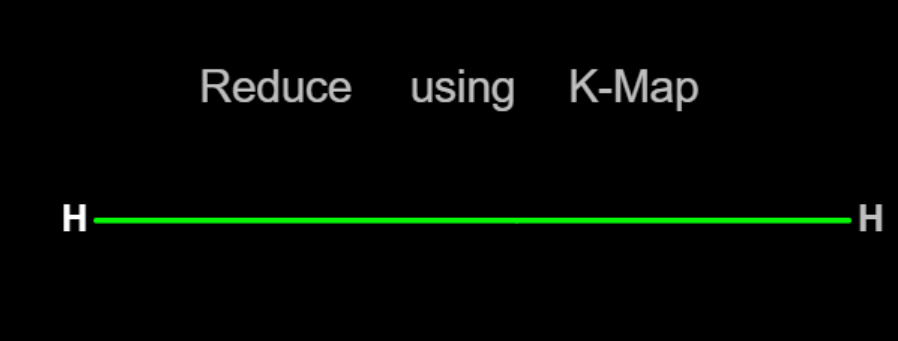
* Problem Description: Reduce the following function x(A,B,C)= ∑m(0,1,3,7)+ ∑d(2,5)



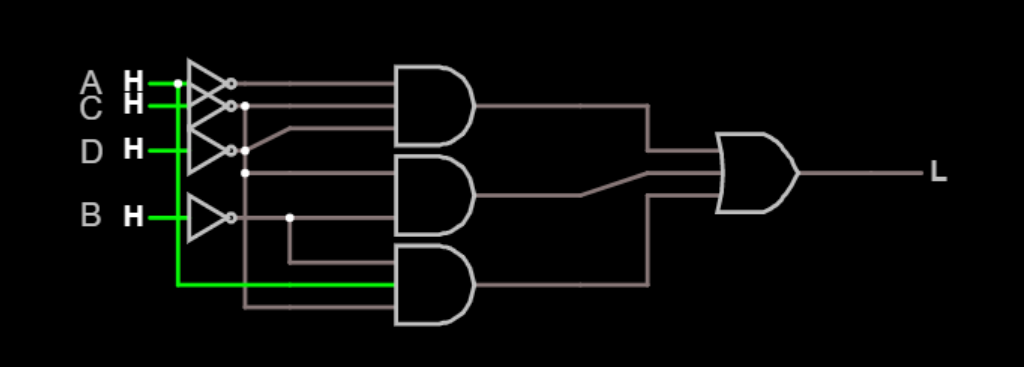
* Problem Description: Simplify the following function using using K-Map  *Y*=*A*¯*B*¯*C*¯ +*A*¯*BC*¯¯+*ABC*¯¯¯+ *A*¯*B*¯*C* +*ABC*​¯¯



* Problem Description: Draw the reduced logic diagram for f(A,B,C,D)= ∑m(5,6,7,12,13)+ ∑d(4,9,14,15)



* Problem Description: Reduce the following function using K-Map *x*=∑*m*(0,1,4,8,9,10)



**THE END**